Si9712DY

PC Card (PCMCIA) Interface Switch—12-V Suspend Capability

Features

- Programmable V_{CC} Ramp
- Smart Switching
- 12-V Sleepmode Compatible
- Extremely Low R_{ON}
- Reverse Blocking Switches
- V_{PP} Programmable to 0, 12-V or V_{CC}
- Safe Power-Up
- Low Power Consumption
- PC Card 3-V/5-V Compatible
- Logic Compatible Inputs
- Single SO-16 Package

Description

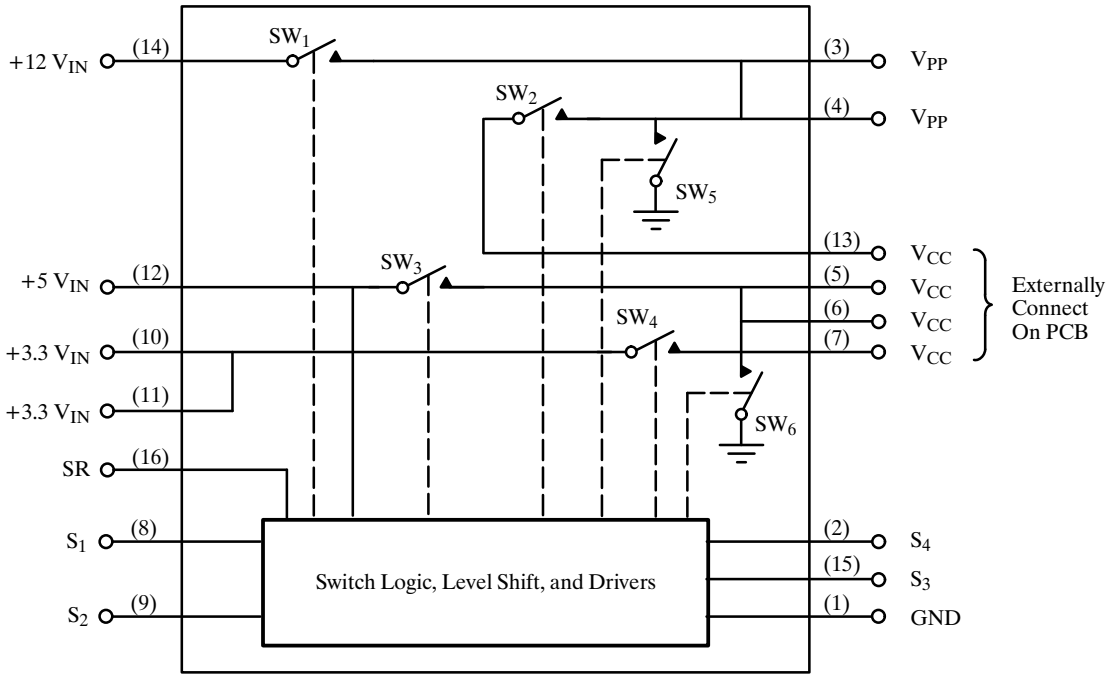
The Si9712DY combines low on-resistance with slow ramp time and smart switching for overall best performance in integrated PC Card interface switches.

The Si9712DY operates off the 5-V supply and has built-in level shifting for gate drive. Internal logic protects against an external control input error that would short 5 V to the 3.3-V supply. This protection logic also allows the Si9712DY to be configured for positive or negative control logic for compatibility with a variety of PC Card controllers. These control inputs are CMOS logic compatible and can be driven to 3.3 V or 5 V.

The Si9712DY complies with the release of the PC Card standard by suppling 0 V, 12 V, and V_{CC} to the V_{pp} output and 0V, 3.3 V, and 5 V to the V_{CC} output. The V_{CC} ramp time is user programmable with an external capacitor connected to the SR pin.

The PC Card switch is packaged in a narrow body SO-16 package and is rated over the industrial temperature range −40 to 85°C.

Functional Block Diagram



This product has been released by Siliconix in November, 1994. Subsequent updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #1328.

Absolute Maximum Ratings

Voltages Referenced to Ground
+12 V_{IN} . . . . . 15 V
+5 V_{IN} . . . . . 7 V
+3.3 V_{IN} [c] . . . . . 7 V
S_1 through S_4 (CMOS Inputs) . . . . . 7 V
I_{OUT} V_{PP}[a] . . . . . 300 mA
All Pins . . . . . −0.5 V
I_{OUT} V_{CC}[b] . . . . . 4 A

PD Max: (T_A = 25°C) . . . . . 2.5 W
(T_A = 85°C) . . . . . 1.0 W
Junction Temperature . . . . . 125°C
Thermal Rating—$R_{\Theta JA}$ . . . . . 40 °C/W

Notes
a. Pins 3, 4 connected together externally.
b. Pins 5, 6, 7, 13 connected together externally.
c. Pins 10, 11 connected together externally.

Recommended Operating Conditions

+12 V_{IN} . . . . . 0 or 12 V ±10%
+5 V_{IN} (must be present) . . . . . 5 V ±10%
+3.3 V_{IN} [c] . . . . . 3.3 V ±10%
C_{SR} . . . . . 33 nF
I_{OUT} V_{PP}[a] . . . . . 150 mA
I_{OUT} V_{CC}[b] . . . . . 2 A

V_{PP} Load Capacitance . . . . . 10 µF Max
V_{CC} Load Capacitance . . . . . 150 µF Max

Notes
a. Pins 3, 4 connected together externally.
b. Pins 5, 6, 7, 13 connected together externally.
c. Pins 10, 11 connected together externally.

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified C_{SR} = 33 nF, +12 V_{IN} = 12 V, +5 V_{IN} = 5 V +3.3 V_{IN} = 3.3 V, Low ≤ 0.8 V, High ≥ 2.2 V		Limits −40 to 85°C Min[b]	 Typ[c]	 Max[b]	Unit
Switch 1							
On-Resistance	R_{ON}	I = 120 mA, +12 V_{IN} = 11.4 V S_3 = S_1 = High S_2 = S_4 = Low	T_A = 25°C			120	mΩ
			T_A = 85°C			145	
Off Current (+12 V_{IN})	I_{OFF}	+12 V_{IN} = 12.6 V S_1 = Low	T_A = 25°C			1	µA
			T_A = 85°C			10	
Switching Time	$t_{SW1(on)}$	S_2 = S_4 = Low, See Figure 1 S_3 = High		50	200	350	µs
	$t_{SW1(off)}$				1.0	10	
Delay Time	$t_{d(on)}$	See Figure 3 S_2 = S_4 = Low		1.0	6	20	ms
	$t_{d(off)}$			0.1	2.9	10	µs
Rise Time	$t_{SW1(on)}$	S_2 = S_4 = Low, S_3 = High See Figure 2		50	150	300	µs
Switch 2							
On-Resistance	R_{ON}	I = 120 mA, S_2 = S_3 = High S_1 = S_4 = Low	T_A = 25°C			150	mΩ
			T_A = 85°C			180	
Switching Time	$t_{SW2(on)}$	S_1 = S_4 = Low, S_3 = High , See Figure 1		50	200	350	µs
	$t_{SW2(off)}$				1.0	10	
Delay Time	$t_{d(on)}$	S_1 = S_4 = Low, See Figure 3		1.0	6	20	ms
	$t_{d(off)}$			0.1	1.7	10	µs
Rise Time	$t_{SW2(on)}$	S_1 = S_4 = Low, S_3 = High See Figure 2		50	150	300	µs

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified C_{SR} = 33 nF, +12 V_{IN} = 12 V, +5 V_{IN} = 5 V +3.3 V_{IN} = 3.3 V, Low ≤ 0.8 V, High ≥ 2.2 V		Limits −40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Switch 3							
On-Resistance	R_{ON}	I = 500 mA, S_3 = High S_1 = S_2 = S_4 = Low	T_A = 25°C			70	mΩ
			T_A = 85°C			95	
Off Current (V_{CC})	I_{OFF}	+5 V_{IN} = 5.5 V, V_{CC} = 0 V S_1 = S_2 = S_3 = Low S_4 = High +3.3 V_{IN} = Open Circuit	T_A = 25°C			1	µA
			T_A = 85°C			10	
Rise Time	$t_{SW3(on)}$	S_1 = S_2 = S_4 = Low, See Figure 2		0.1	1.7	10	ms
Fall Time	$t_{SW3(off)}$			3	30	50	
Switch 4							
On-Resistance	R_{ON}	I = 500 mA, S_4 = High S_1 = S_2 = S_3 = Low	T_A = 25°C			50	mΩ
			T_A = 85°C			70	
Off Current (+3.3 V_{IN})	I_{OFF}	+3.3 V_{IN} = 3.6 V, S_1 = S_2 = S_3 = S_4 = Low	T_A = 25°C			1	µA
			T_A = 85°C			10	
Rise Time	$t_{SW4(on)}$	S_1 = S_2 = S_3 = Low, See Figure 2		0.1	0.9	10	ms
Fall Time	$t_{SW4(off)}$			3	20	40	
Switch 5							
On-Resistance	R_{ON}	I = 2 mA, S_1 = S_2 = Low	T_A = 25°C		235	400	Ω
			T_A = 85°C		325	550	
Switch 6							
On-Resistance	R_{ON}	I = 2 mA, S_3= S_4 = Low	T_A = 25°C		140	400	Ω
			T_A = 85°C		200	500	
Power Supply							
+5 V_{IN} Current Input (on)	$I_{+5VIN(1)}$	S_1 = S_4 = 0 V, S_2 = S_3= 3 V			20	50	µA
	$I_{+5VIN(2)}$	S_1 = S_4 = 3 V, S_2 = S_3 = 0V			20	50	
+5 V_{IN} Current Input (off)	$I_{+5VIN(3)}$	S_1 = S_2 = S_3 = S_4 = 0 V			<1	10	
Switch Control Inputs							
Input Voltage High	$V_{I(H)}$	+5 V_{IN} = 5.5 V		2.2	1.8		V
		+5 V_{IN} = 4.5 V		2.2	1.6		
Input Voltage Low	$V_{I(L)}$	+5 V_{IN} = 5.5 V			1.6	0.8	
		+5 V_{IN} = 4.5 V			1.4	0.8	
Input Current High	$I_{I(H)}$	S_1 through S_4 = 5 V				1.0	µA
Input Current Low	$I_{I(L)}$	S_1 through S_4 = GND		−1.0			

Notes
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Timing Waveforms

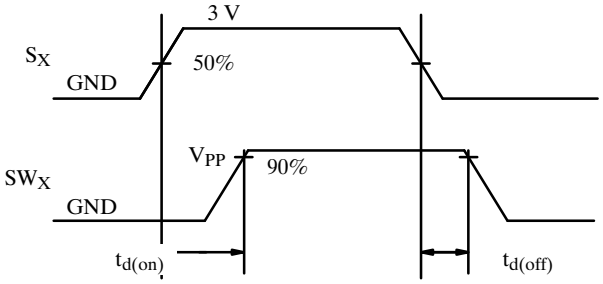


Figure 1. V_{PP} Switch Delay

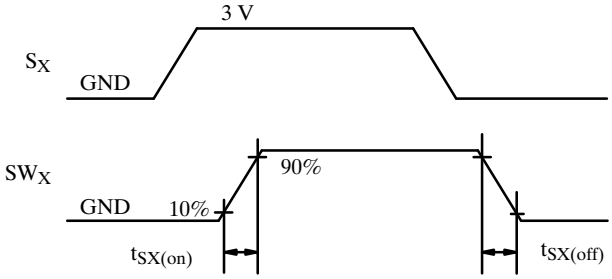


Figure 2. Switch Ramp

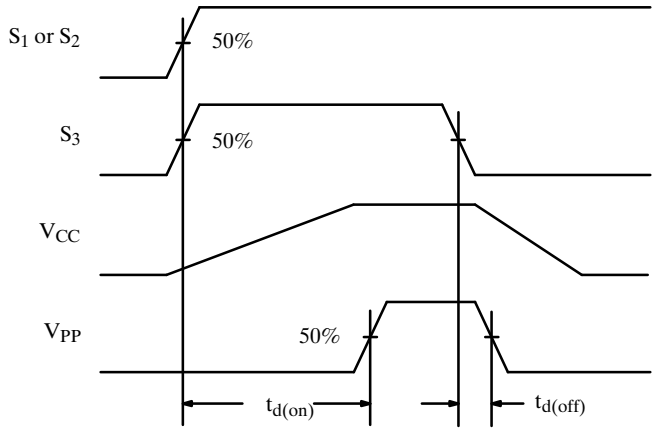
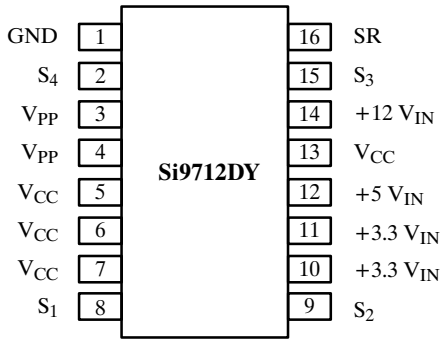


Figure 3. Delay from S_1 or S_2 to V_{PP} Power-up

Pin Configuration/Pin Description

SO-16



Top View

Note: Pins 5, 6, 7, and 13 must be connected in the PCB for correct operation.

Pin Number	Function	Description
1.	GND	Ground connection.
2	S_4	Control input for selecting +3.3 V_{IN} to V_{CC}. The PC Card terminology for this pin is $V_{CC}\_EN_0$.
3, 4	V_{PP}	Program and peripheral voltage to PC Card slot.
5, 6, 7, 13	V_{CC}	Supply voltage to slot.
8	S_1	Control input for selecting +12 V_{IN} to V_{PP}. The PC Card terminology for this pin is $V_{PP}\_EN_1$.
9	S_2	Control input for selecting V_{CC} to V_{PP} . The PC Card terminology for this pin is $V_{PP}\_EN_0$.
10, 11	+3.3 V_{IN}	+3.3-V supply.
12	+5 V_{IN}	+5-V supply.
14	+12 V_{IN}	+12-V supply.
15	S_3	Control input for selecting +5 V_{IN} to V_{CC}. The PC Card terminology for this pin is $V_{CC}\_EN_1$.
16	SR	Slew rate control pin, capacitor to GND defines programmable ramp time.

Truth Table[b]

S_1	S_2	S_3	S_4	Switch 1[a]	Switch 2[a]	Switch 3	Switch 4	Switch 5	Switch 6
0	0	0	0	Off	Off	Off	Off	On	On
0	0	0	1	Off	Off	Off	On	On	Off
0	0	1	0	Off	Off	On	Off	On	Off
0	0	1	1	Off	Off	Off	Off	On	On
0	1	0	0	Off	Off	Off	Off	On	On
0	1	0	1	Off	On	Off	On	Off	Off
0	1	1	0	Off	On	On	Off	Off	Off
0	1	1	1	Off	Off	Off	Off	On	On
1	0	0	0	Off	Off	Off	Off	On	On
1	0	0	1	On	Off	Off	On	Off	Off
1	0	1	0	On	Off	On	Off	Off	Off
1	0	1	1	Off	Off	Off	Off	On	On
1	1	0	0	Off	Off	Off	Off	On	On
1	1	0	1	On	Off	Off	On	Off	Off
1	1	1	0	On	Off	On	Off	Off	Off
1	1	1	1	Off	Off	Off	Off	On	On

Notes
a. Turn on of switch 1 and 2 are internally delayed until after V_{CC} is valid. See Figure 3.
b. Shaded lines are error conditions for PC Card applications, however, switches default to the states shown.

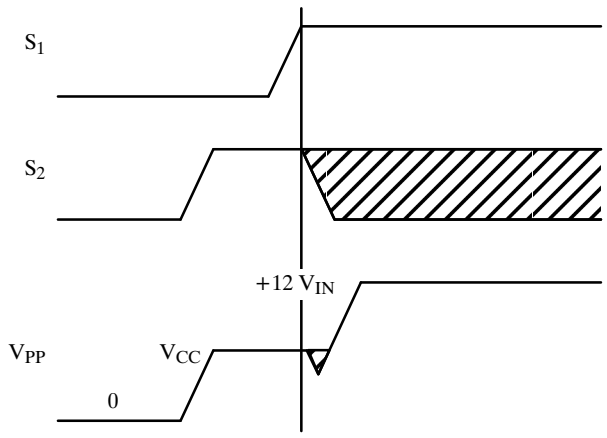
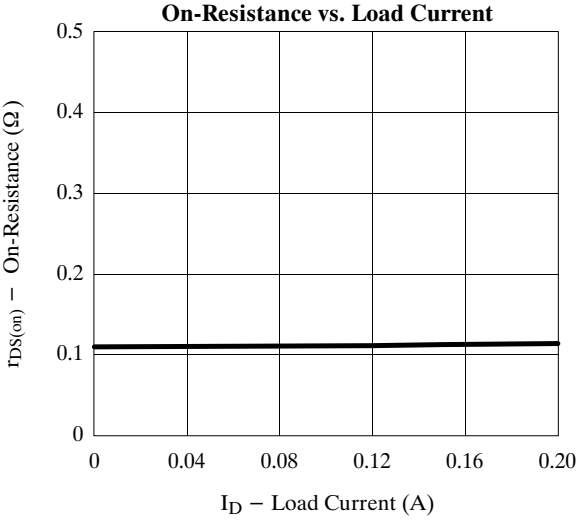


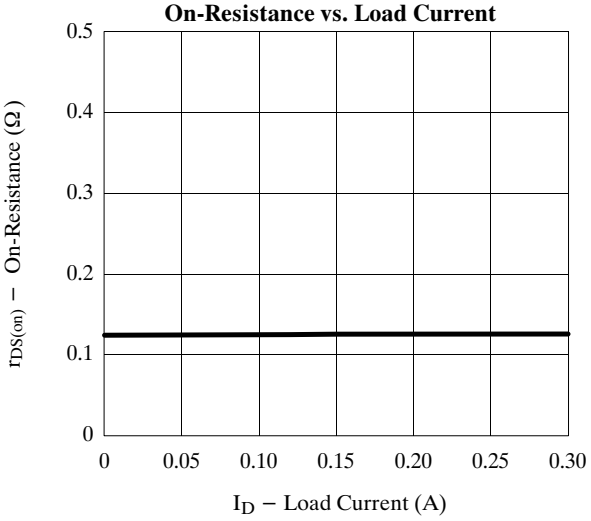
Figure 4. Break-Before-Make of SW_1 and SW_2

Typical Characteristics (25°C Unless Otherwise Noted)

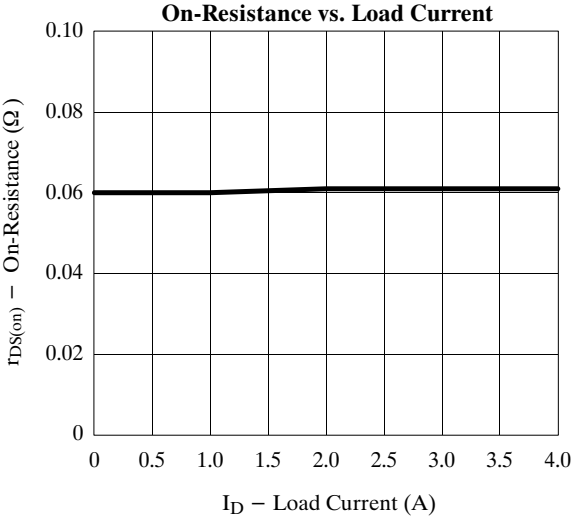
Switch 1
On-Resistance vs. Load Current



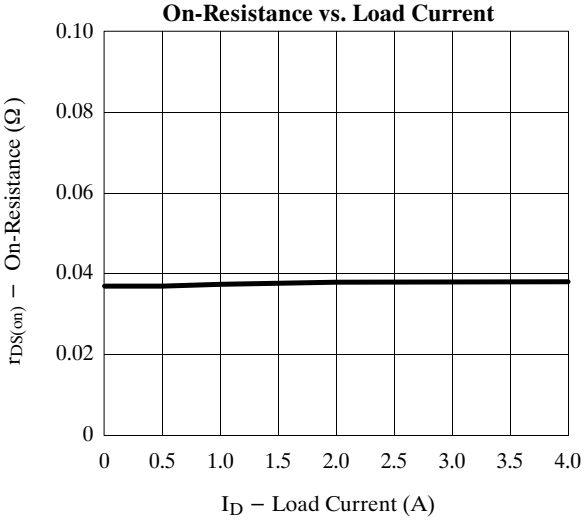
Switch 2
On-Resistance vs. Load Current



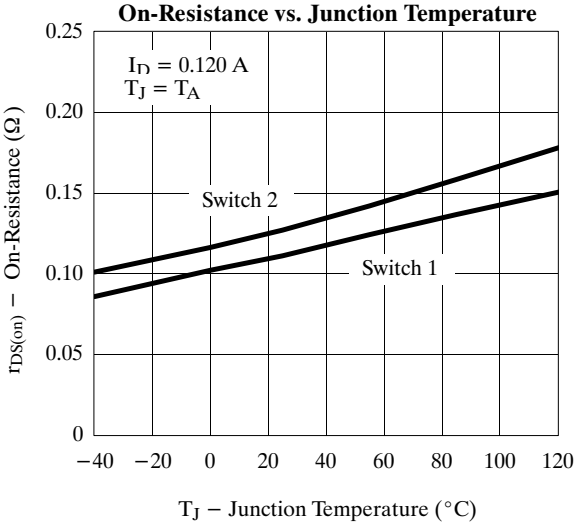
Switch 3
On-Resistance vs. Load Current



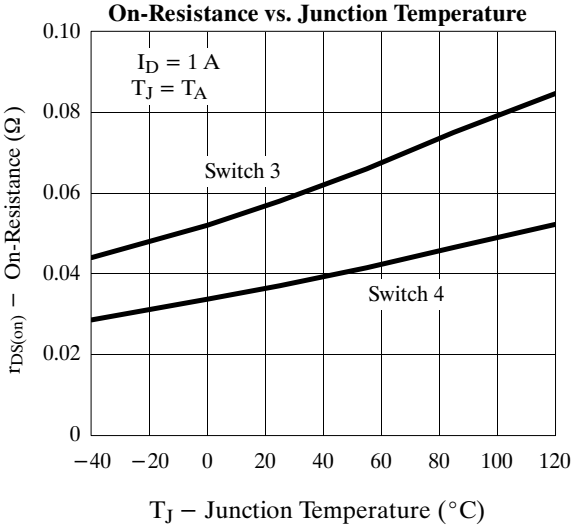
Switch 4
On-Resistance vs. Load Current



On-Resistance vs. Junction Temperature

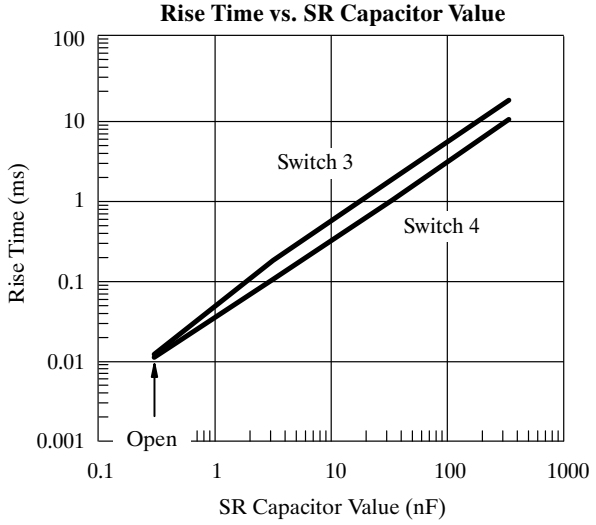


On-Resistance vs. Junction Temperature

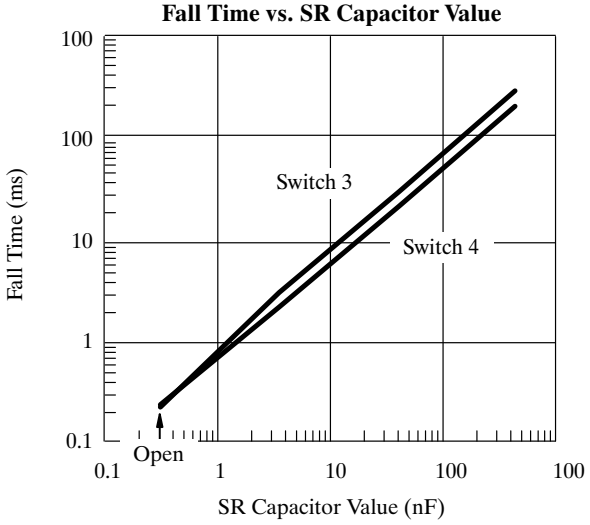


Typical Characteristics (25°C Unless Otherwise Noted)

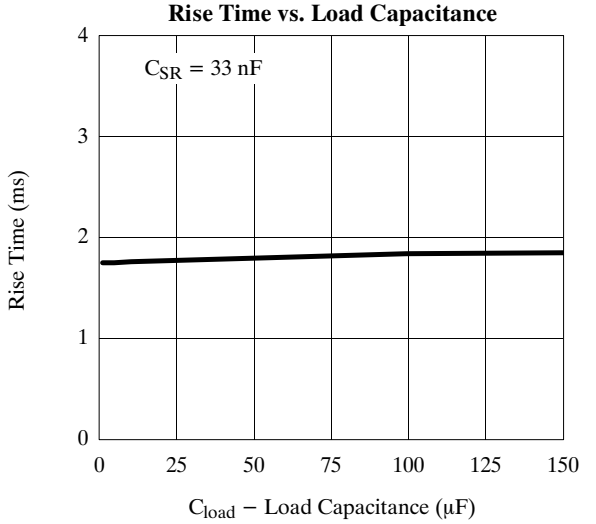
Rise Time vs. SR Capacitor Value



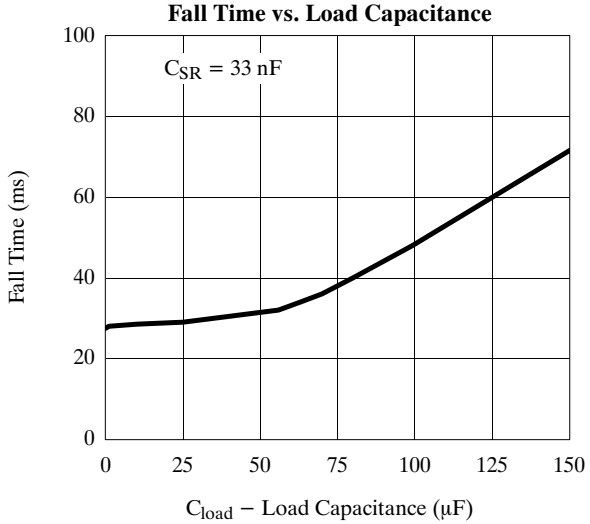
Fall Time vs. SR Capacitor Value



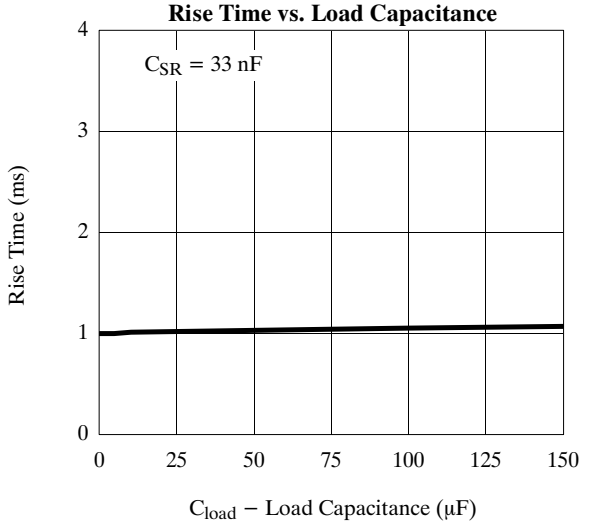
Switch 3
Rise Time vs. Load Capacitance



Switch 3
Fall Time vs. Load Capacitance



Switch 4
Rise Time vs. Load Capacitance



Switch 4
Fall Time vs. Load Capacitance